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Review

An introduction to the Medipix family ASICs

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ABSTRACT

The first Medipix chip which aimed at permitting single photon counting on a sizable matrix of pixels was developed in the mid-1990's. In the following 20 years two families of chips have evolved from that initial effort. The Medipix photon counting family of chips comprises Medipix, Medipix2 and Medipix3. A 4th generation chip, Medipix4, is under development. The Timepix chips were initially more aimed at single particle detection and that family comprises Timepix, the most recent Timepix2 chip (introduced in this Special Issue) and Timepix3. The 4th generation Timepix4 is also under development and a first version will be produced in 2019. This paper seeks to provide a brief introduction to the various members of the Medipix family and provide references to more detailed descriptions already available in the literature.

1. Introduction

Pixel detectors were first developed for use in High Energy Physics tracking detectors (Heijne, 2019). The 2-dimensional pixel detector geometry was a natural evolution from the projective linear arrays of silicon strip detectors and ASICs which were developed in the 80's and 90's for particle tracking. High density bump bonding combined with the increasing transistor density provided by commercial CMOS processes were the technical developments which permitted the 'dream' of hybrid pixel detectors (Heijne et al., 1988) to become a reality. A particularly fortuitous side effect of the close integration of CMOS amplifier and pixelated sensor diode was the inherently low input capacitance which permitted the design of low noise and low power pre-amp and shaper circuits which in turn allowed noise hit free particle detection even with relatively fast shaping times. Another side effect was the benefit of having small pixels with respect to the detector thickness which allows the electronics to be sensitive to only one type of carrier when this is close to the collection electrodes. This fact can be exploited in high-Z sensors to be sensitive to the more mobile electrons and to be insensitive in the signal generation to holes which are are susceptible to trapping. We have also shown that this "small pixel effect" combined with an excellent time resolution, has been exploited to track the particles inside the semiconductor sensor volume as in a Time Projection Chamber.

In HEP experiments tracking detectors are typically required to save hit information until some external 'trigger' initiates readout of what should be an interesting event and a rectangular pixel shape is often preferred as it provides a precise coordinate in the direction of a prevailing magnetic field. The first Medipix chip (Campbell et al., 1998) aimed to provide noise hit free particle imaging by incorporating a counter on each pixel and combining the sensitive pixel matrix with a shutter-based camera-type of readout. Particles are counted on-pixel when an electronic shutter is high and the counters are read out when the shutter is low. Evidently a square shape of pixel was preferred for such applications. Since then the Medipix family of pixel detector readout chips has grown in size and complexity. A recent review of the Medipix and Timepix ASICs can be found here (Ballabriga et al., 2018). In that review the design of the chips is explained in more detail and a number of other related chip developments are discussed. This brief article intends to provide the reader of this Special Issue with a succinct summary of the Medipix and Timepix readout chips which have been developed adding the recent Timepix2 chip (Wong, 2019) and including the specifications for the Medipix4 and Timepix4 readout chips.

2. The Medipix chips

Table 1 summarizes the characteristics of the Medipix chips. Each device is introduced briefly here. The original Medipix or Photon Counting Chip (PCC) which was fabricated in 1997 was composed of an array of 64 x 64 identical square pixels on a pitch of 170 μm (Campbell et al., 1998). Each pixel has a charge sensitive pre-amplifier with a gain of ~30mV/ke$^-$. The pre-amp is followed by a comparator with 3 bits of threshold adjust and a 15-bit pseudo random counter. This counter is reconfigured as a shift register during readout. The electrical noise per

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Table 1
A list of the main characteristics of the Medipix chip family.

	Medipix	Medipix2	Medipix3	Medipix4
Tech. node (nm)	1000	250	130	130
Year	1997	2005	2013	2021
Pixel size (μm)	170	55	55	70/140
# pixels (x x y)	64 x 64	256 x 256	256 x 256/128 x 128	320 x 320/ 1690 x 160
Charge summing mode	No	No	Yes	Yes
Readout architecture	Sequential R/W	Sequential R/W	Sequential or continuous R/W	Sequential or continuous R/W
Number of sides for tiling	0	3	3	4

channel is ~80 e^- rms and the minimum operating threshold after adjustment is ~2000 e^-. The on-chip detection circuitry was surrounded by relatively wide metal lines bringing power to the pixel matrix from all sides prohibiting to the abutment of chips to form larger detection areas.

The Medipix2 chip (Llopart et al., 2002) underwent several iterations from ~2002 until ~ 2005 with the final version being called MPIX2MXRV2. It was designed in a 250 nm CMOS process and is composed of a matrix of 256 x 256 identical square pixels on a pitch of 55 μm. Each pixel has a pre-amp with a measured gain of 10 mV/ke^- and a window discriminator with high and low thresholds which can be tuned with 3 bits of adjustment each. The minimum operating threshold is ~800 e^-. Each pixel has a 14-bit counter with overflow protection logic which stops the counter when it reaches a value of 11810. The chip is designed to minimise the dead area on 3 sides permitting multiple chips to be connected to a single sensor.

The Medipix3 chip also underwent a few iterations with the final version call Medipix3RX (Ballabrigaet al., 2013) being produced in 2013. It is designed in a 130 nm CMOS process and implements a novel charge summing and allocation scheme which is intended to overcome the detrimental effects of charge sharing in the detector on the spectroscopic imaging performance of the chip. Charge diffusion in the detector during charge collection and fluorescence in high-Z semiconductor materials are at the origin of the charge sharing. In the Medipix3 chips simultaneous hits within a local region of pixels are detected and compared with each other and the pixel with the highest local charge deposition is the pixel identified to record that hit. In parallel with this process local charge sums are made at the corners of each pixel and the allocated pixel selects its corner with the biggest charge sum. This process can be carried out on detector pixels at a pitch of 55 μm therefore collecting over a total surface area of 110 × 110 μm^2 or on detector pixels at a pitch of 110 μm (only one electronics pixel in 4 is connected to the sensor) permitting charge to be collected over an area of 220 x 220 μm^2. The Medipix3 chip has 2 counters per 55 μm pixel. These can be configured to permit continuous reading and data collection (1 threshold per pixel of 55 μm, 4 thresholds per pixel of 110 μm). If required the charge summing and allocation functionality can be disabled permitting single pixel mode. Like its predecessor, Medipix2, it is read out on one side only permitting tiling of 2 x n chips on a single large sensor. The Medipix3 included the possibility to dice off the wire bonding pads to allow connection using Through Silicon Via (TSV). This allows to minimise the inactive area of the system. The TSV connection was prototyped in this design (Campbellet al., 2016).

The Medipix4 chip is still in the design phase. It is being designed in a 130nm CMOS process. It will be composed of a matrix of 32032 x 320 pixels on a pitch of 70 μm and will be programmable to be connected to a sensor with a pixel pitch of 140 μm. A charge summing and allocation scheme similar to that implemented in Medipix3 will permit charge summing over an area of either 140 × 140 μm^2 or 280 × 280 μm^2 depending on the sensor pixel pitch. Each 70 μm pixel will have 4 counters to permit up to 2 charge summing thresholds in continuous read/write mode. When connected to a sensor with 140 μm pitch up to 8 thresholds in charge summing mode will be available. The maximum count rate is expected to be ~100 × 10^6 photons/mm^2/sec in charge summing mode. The chip will be designed to be tile-able on 4 sides. In order to achieve this the readout ASIC pixels will be slightly rectangular in shape. This allows for space at the top, middle and bottom of the readout matrix where IO and control logic can be placed. A fan-in from the top metal layer containing a uniform matrix of 320 x 320 bump bonding pads to the readout pixels is used to redistribute the signals from the sensor pads to the location where the readout pixels are laid out (the readout pixels being smaller than the sensor pixels). Connection to the back of the readout chips is achieved using Through Silicon Vias in ways described in (Campbellet al., 2016).

3. The Timepix chips

Table 2 summarizes the characteristics of the Timepix chips. Each member of the family is introduced briefly here.

The Timepix chip (Llopart et al., 2007) was designed in 2005 and is based very much on the Medipix2 chip. Therefore, the pixel size, matrix size and readout scheme are identical to Medipix2. Instead of merely counting hits within a given threshold window, the pixels of the Timepix chip can be programmed into one of 3 modes: (a) hit counting mode (b) Time of Arrival (ToA) mode (c) Time-over-Threshold (ToT) mode. The on-pixel 14-bit counter is identical to that of Medipix2.

The Timepix2 chip (Wong, 2019) was only recently produced. This chip intends to replace Timepix and is aimed particularly at space applications where measurements in mixed radiation fields are foreseen. Like Timepix is it composed of a matrix of 256 x 256 pixels on a pitch of 55 μm. However, being designed in a 130 nm process it has more sophisticated capabilities. The front-end has an optional adaptive gain circuit (in hole collection only) which extends the linear dynamic range sensitivity to ~ 1 Me^- per pixel. The chip is highly programmable with 28 bits per pixel which can be configured as counters of varying depths in different modes for different purposes. When the chip is programmed for sequential read/write (being insensitive during readout) ToT and ToA are recorded simultaneously at the pixel level (10-bit ToT and 18-bit ToA or 14-bits for each of ToT and ToA). However, the counters can be also be configured for continuous read/write where, ToT, ToA or the hit counts are recorded. It is possible to power down individual pixels where only a particular region of interest is to be read out or where larger pitch pixel sensors are used.

Timepix3 (Poikelaet al., 2014) was fabricated in 2014 in a 130 nm CMOS process. The pixel matrix size and dimensions are identical to Timepix, Timepix2, Medipix2 and Medipix3. There are a number of important innovations in Timepix3. It was the first chip in the family to record simultaneously ToT (10 bits) and ToA (up to 18 bits). There is a special super-pixel architecture which incorporates a VCO circuit (started by the discriminator firing and stopped on the next rising clock edge) permitting time stamping within a time bin of 1.56 ns. The readout architecture is novel too – when a pixel is hit it is the pixel itself which sends its data down the column and then off chip. This is the first fully functioning pixel readout chip with a data driven readout architecture. This provides a great deal of flexibility compared to devices with frame-based readouts but at the expense of increased complexity in the readout system.

Timepix4 is designed in 65 nm CMOS and will be produced in 2019. Like Medipix4 it will be designed to be tile-able on 4 sides. It will comprise of a matrix of 448 x 512 pixels with an on-sensor pitch of 55 μm. It will also have a data driven readout scheme sending out ToT and ToA data but with an improved time stamp bin of 200 ps. The chip also has a photon counting mode. In that mode a single threshold is available and simultaneous read/write can be used with counts rate of up to ~800 Ghits/cm^2/sec.

Table 2
A list of the main characteristics of the Timepix chip family.

	Timepix	Timepix2	Timepix3	Timepix4
Tech. node (nm)	250	130	130	65
Year	2005	2018	2014	2019
Pixel size (μm)	55	55	55	55
# pixels (x x y)	256 x 256	256 x 256	256 x 256	448 x 512
Time bin (resolution)	10ns	10ns	1.6ns	200ps
Readout architecture	Frame based (sequential R/W)	Frame based (sequential or continuous R/W)	Data driven or Frame based (sequential R/W)	Data driven or Frame-base (sequential or continuous R/W)
Number of sides for tiling	3	3	3	4

4. Summary

In this Special Issue there are reports on many of the applications to which the Medipix and Timepix chips have been used. With each new generation we have sought to bring the field one step forward by adopting the more downscaled CMOS processes and developing new approaches to pixel readout. The design of the chips is a major factor in the success story but it would not have been possible without the continuous input and support (scientific, technical and financial) and enthusiasm of the members of the various Medipix Collaborations.

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References

Ballabriga, R., Campbell, M., Llopart, X., 2018. Asic developments for radiation imaging applications: the medipix and timepix family. Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip. 878, 10–23. July 2017.

Ballabriga, R., et al., 2013. The medipix3RX: a high resolution, zero dead-time pixel detector readout chip allowing spectroscopic imaging. J. Instrum. 8 (2).

Campbell, M., Heijne, E.H.M., Meddeler, G., Pernigotti, E., Snoeys, W., 1998. A readout chip for a 64 x 64 pixel matrix with 15-bit single Photon Counting. IEEE Trans. Nucl. Sci. 45 (3), 751–753.

Campbell, M., et al., 2016. Towards a new generation of pixel detector readout chips. J. Instrum. 11 (1).

Heijne, E.H.M., 2019. History and future of radiation imaging with single quantum processing pixel detectors. Radiat. Meas. This issue.

Heijne, E.H.M., Jarron, P., Olsen, A., Redaelli, N., 1988. The silicon micropattern detector: a dream? Nucl. Instrum. Methods Phys. Res. A 273 (2–3), 615–619.

Llopart, X., Campbell, M., Dinapoli, R., San Segundo, D., Pernigotti, E., 2002. Medipix2: a 64-k pixel readout chip with 55-um square elements working in single photon counting mode. IEEE Trans. Nucl. Sci. 49 I (5), 2279–2283.

Llopart, X., Ballabriga, R., Campbell, M., Tlustos, L., Wong, W., 2007. Timepix, a 65k programmable pixel readout chip for arrival time, energy and/or photon counting measurements. Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip. 581 (1–2), 485–494. SPEC. ISS.

Poikela, T., et al., 2014. Timepix3: a 65K channel hybrid pixel readout chip with simultaneous ToA/ToT and sparse readout. J. Instrum. 9 (5), C05013.

Wong, W.S., 2019. Introducing Timepix2, a frame-based pixel detector readout ASIC measuring energy deposition and arrival time. Radiat. Meas. This issue.